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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,937	01/15/2002	Gen Nakamura	03560.002982	1497

5514 7590 02/13/2004

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EXAMINER	
FRANK, ELLIOT L	

ART UNIT	PAPER NUMBER
2125	8

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/044,937	Applicant(s) NAKAMURA, GEN	
	Examiner Elliot L Frank	Art Unit 2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED FINAL ACTION

Response to Amendment

1. The following response is a FINAL office action in response to applicant's amendment (A) filed 2 February 2004.
2. The applicant's corrections or explanations with regard to items 1-4 of the previous office action have been considered and are accepted.
3. Claims 1-20 remain pending in the application. Claims 1,10 and 19 have been amended. Claims 21-25 have been withdrawn due to the previous restriction requirement.

Response to Arguments

4. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection that were perpetuated by the applicant's amendments.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6,8-12,14,15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayser (USPN 6,333,602 B1) in view of Hayata (USPN 5,726,739 A).

The limitations of the aforementioned claims, and the applicable citations in Kayser, are as follows:

1. A semiconductor manufacturing apparatus comprising:

a light source (column 4, lines 42-50); and

a lighting device, said lighting device comprising

(i) an electrical power source unit for supplying electricity to said light source, and

(ii) a starter unit for lighting said light source, wherein said starter unit has a metal piece for connecting said lighting device to said light source (requirements (i) and (ii) are read at column 5, lines 13-25), [and a unit for moving the metal piece and the connected light source relative to the connected lighting device].

2. A semiconductor manufacturing apparatus according to claim 1, wherein said light source is a discharge lamp (column 4, lines 42-50).

3. A semiconductor manufacturing apparatus according to claim 1, wherein said metal piece is disposed at a side wherein high voltage is applied for lighting said light source (column 5, lines 13-25, wherein the connection between the light source 10 and the socket 114 / ballast 113 is described).

4. A semiconductor manufacturing apparatus according to claim 1, further comprising a mechanism for integrally driving said light source and said lighting

device (column 5, lines 13-25, wherein all of the aforementioned devices are integrated within housing 102).

6. A semiconductor manufacturing apparatus according to claim 1, wherein said light source and said lighting device are disposed within a single housing (column 5, lines 13-25, wherein all of the aforementioned devices are integrated within housing 102).

8. A semiconductor manufacturing apparatus according to claim 6, wherein the temperature of said light source and said lighting device is adjusted using air of the ambient atmosphere from outside said housing, taken into said housing from a single air intake and being subjected to temperature adjustment with a single temperature adjusting means (column 5, lines 31-41).

9. A semiconductor manufacturing apparatus according to claim 8, wherein said light source and said lighting device are subjected to temperature adjustment in the order of said lighting device first and then said light source, using the taken in air (Obvious in view of Kayser figures 2A and 3 wherein the cooling device, in this case a fan 110, is disposed to blow air over a ballast 113 before the lighting source 10).

Hayata, analogous to Kayser in that both describe light source control systems (Hayata, column 1, line 66-column 2, line 21), is referenced here to further support Kayser in demonstrating that Kayser, a generic lighting system (Kayser, column 1, lines 8-10), has well known application to a semiconductor manufacturing process (Hayata, column 1, lines 7-12). Claim 1 also requires that the light source be connected to said starter by "a metal piece". While Kayser anticipates a multitude of

light sources (Kayser, column 4, lines 42-50) a light source with a single metal connection was not mentioned. Hayata demonstrates that such a light source configuration was well known in the art at the time the invention was made (column 3, lines 45-56 and figure 1 wherein the light source, item 1, has a single point of connection). Hayata also reads on the newly amended limitations of claim 1 wherein a unit is provided to move the light source relative to the connected lighting device (column 5, lines 32-45).

The limitations of claim 5 are read in Hayata as follows:

5. A semiconductor manufacturing apparatus according to claim 1, further comprising means for changing the positional relation between said light source and an optical element disposed near said light source (column 4, line 66-column 5, line 9).

Claims 10-12,14,15-17 have the same functional limitations as claims 1,2,6,3,4,5 and 8 respectively. Therefore, these claims are obvious in view of the same citations in the combined references.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the features of Hayata with the Kayser system to have provided a system that could have corrected illuminance non-uniformness, asymmetric with respect to the optical axis, formed or to be formed on the image plane with the change of the light intensity distribution (Hayata, column 1, line 38-column 2, line 21).

7. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayser (USPN 6,333,602 B1) in view of Hayata (USPN 5,726,739 A) as applied to claims 1 and 10 above, and further in view of Hayama et al. (USPN 6,104,204 A).

Claims 7 and 13 depend from claims 1 and 10 respectively. Claims 1 and 10 have been shown to be obvious in view of Kayser and Hayata.

While the combined references make obvious a light source used in a semiconductor processing application, they do not specifically read on the additional limitations of claim 7:

7. A semiconductor manufacturing apparatus according to claim 6, wherein said housing has outer walls provided with electromagnetic shielding and has a configuration of copper wire mesh sandwiched between thermal insulating material, said copper wire mesh being grounded.

Hayama et al., analogous to the previously combined references in that they all are applicable to a semiconductor manufacturing process tools (Hayama et al., column 1, lines 5-17), reads on the additional requirements of claim 7 at column 8, lines 28-37 and column 14, lines 13-24, wherein it describes a structure meeting the requirements of claim 7.

Claim 13 has the same functional limitations as claim 7, and therefore is obvious in view of the same citations in the combined references.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the elements of Hayama et al. into the combined Kayser and Hayata references to have provided an enclosure that

provides both electromagnetic and thermal shielding (Hayama et al., column 8, lines 28-37).

8. Claims 19 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Kayser (USPN 6,333,602 B1) in view of Hayata (USPN 5,726,739 A) as applied to claims 1 and 10 above, and further in view of Sepe, JR. (US 2001/0047213 A1).

Claim 19 includes the base functional limitations of claim 10 with the additional requirements of network and maintenance information transmitted on said network. The aforementioned combination, while making obvious a light source control apparatus, does not read specifically on the additional limitations of claims 19 and 20 as follows:

19. A semiconductor manufacturing apparatus in which a computer having a display, a network interface, and networking software provides data communication of maintenance information through a computer network, said semiconductor manufacturing apparatus comprising a lamp box including (the limitations of claim 10).

20. A semiconductor manufacturing apparatus according to claim 19, wherein said networking software provides, on said display, a user interface for accessing a maintenance database which is provided by a vendor or user of said semiconductor manufacturing apparatus and which is connected to an external network outside of a plant wherein said semiconductor manufacturing apparatus is installed, thereby enabling information to be obtained from said database via said external network.

Sepe JR., analogous to the aforementioned combined references in that all of them are electronic control applications (Sepe, JR., page 1, paragraph 0003), reads on the additional limitations of claims 19 and 20 at page 3, paragraph 0053, wherein it discusses remote monitoring including the transmission of maintenance information.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the elements of Sepe, JR. into the previously combined references to have provided a virtual presence between geographically remote users and hardware platforms for multiple operations including technical support and remote servicing (Sepe, JR., page 1, paragraph 0014).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

   USPN 5,700,084 A – Yasukawa et al. – Light source positioning

   USPN 6,064,468 A – Sakaguchi – Light source positioning

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elliot L Frank whose telephone number is (703) 305-5442. The examiner can normally be reached on M-F 7-4:30, 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P Picard can be reached on (703) 308-0538. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ELF – February 9, 2004

LEO PICARD
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